

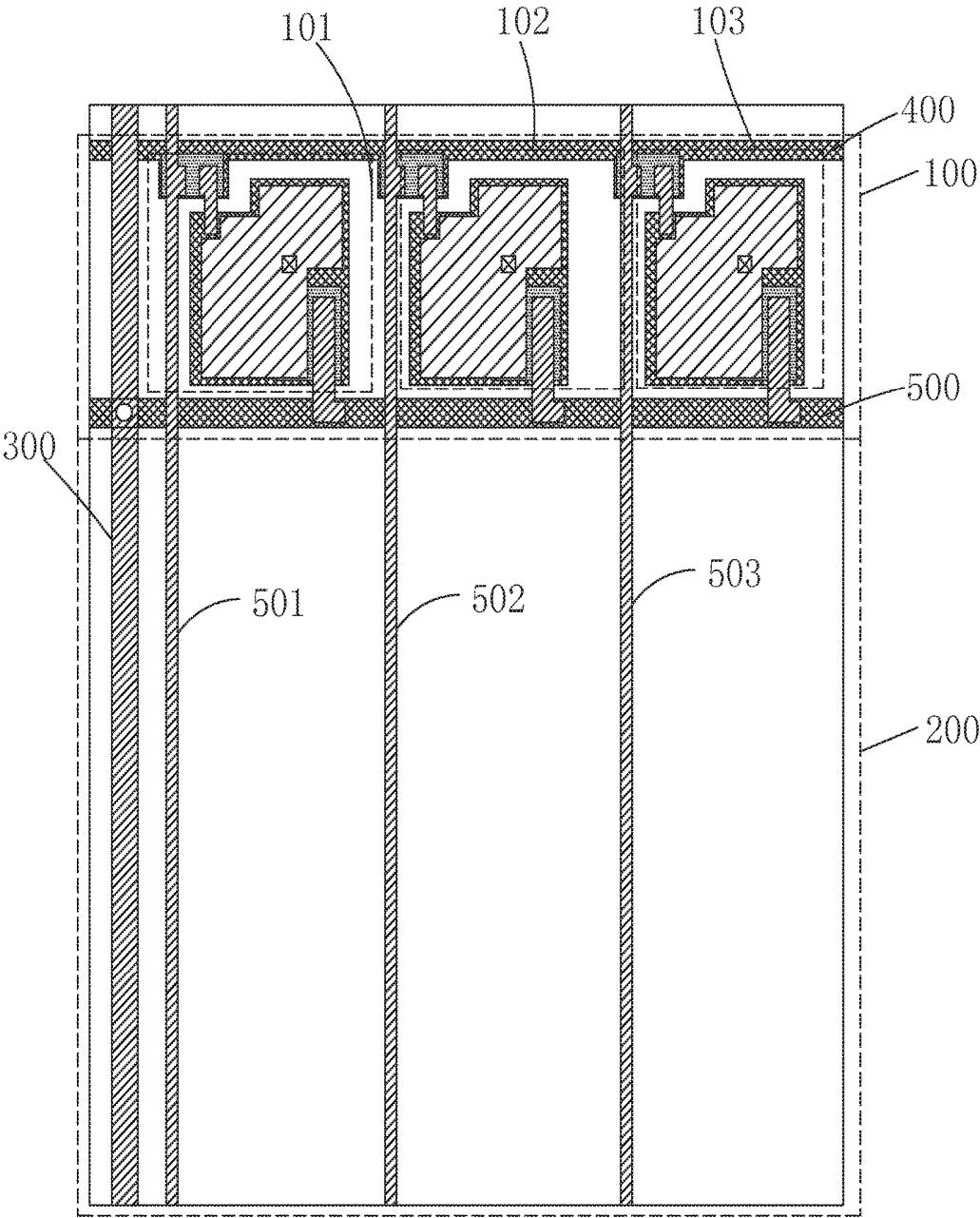


Fig. 1

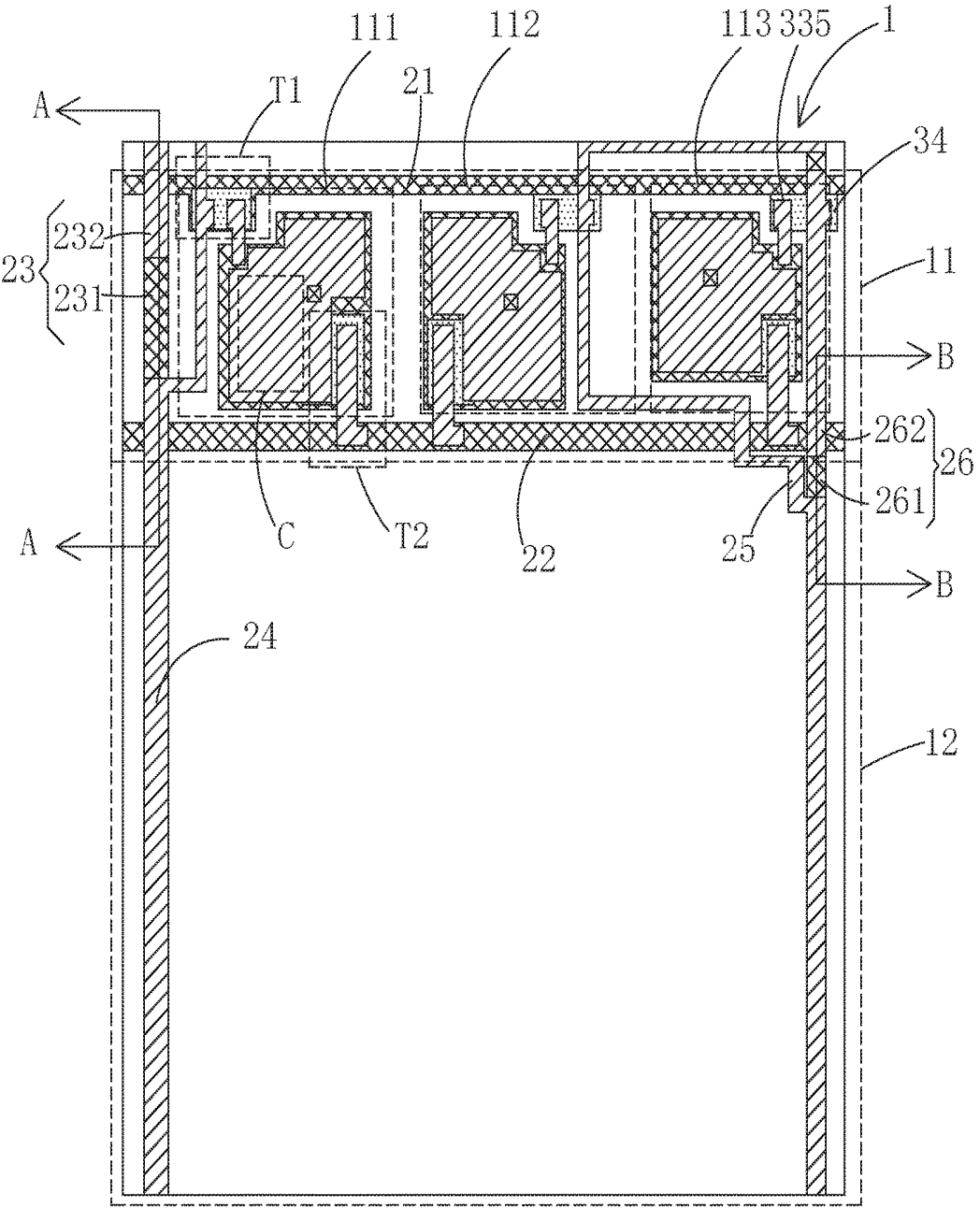


Fig. 2

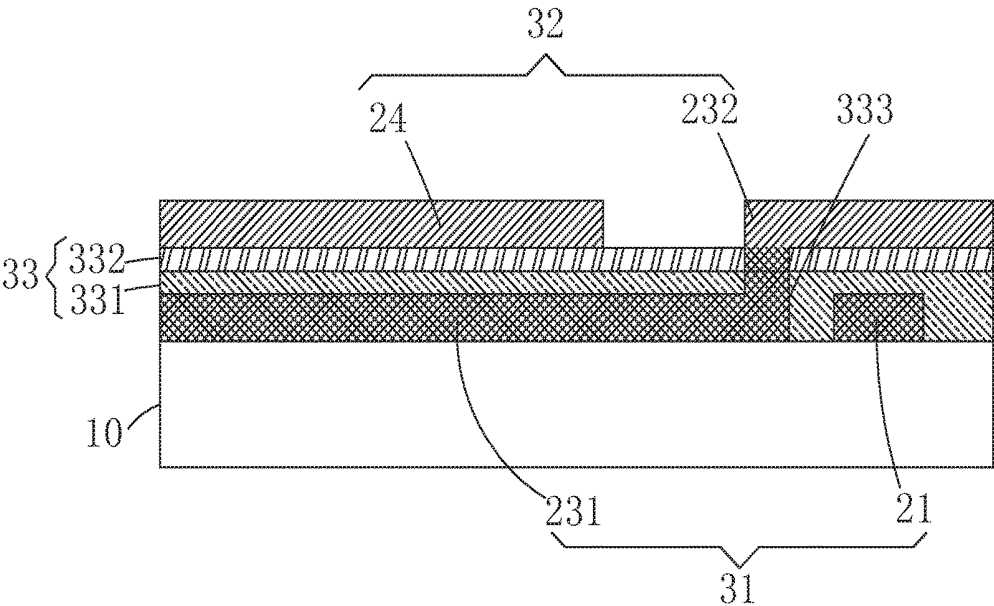


Fig. 3

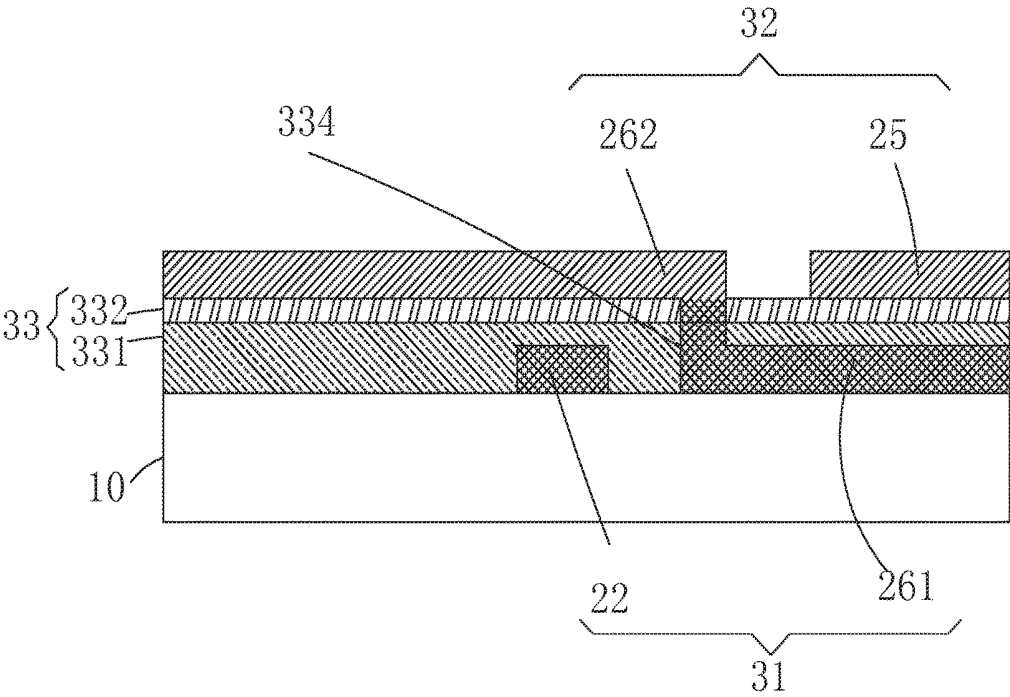


Fig. 4

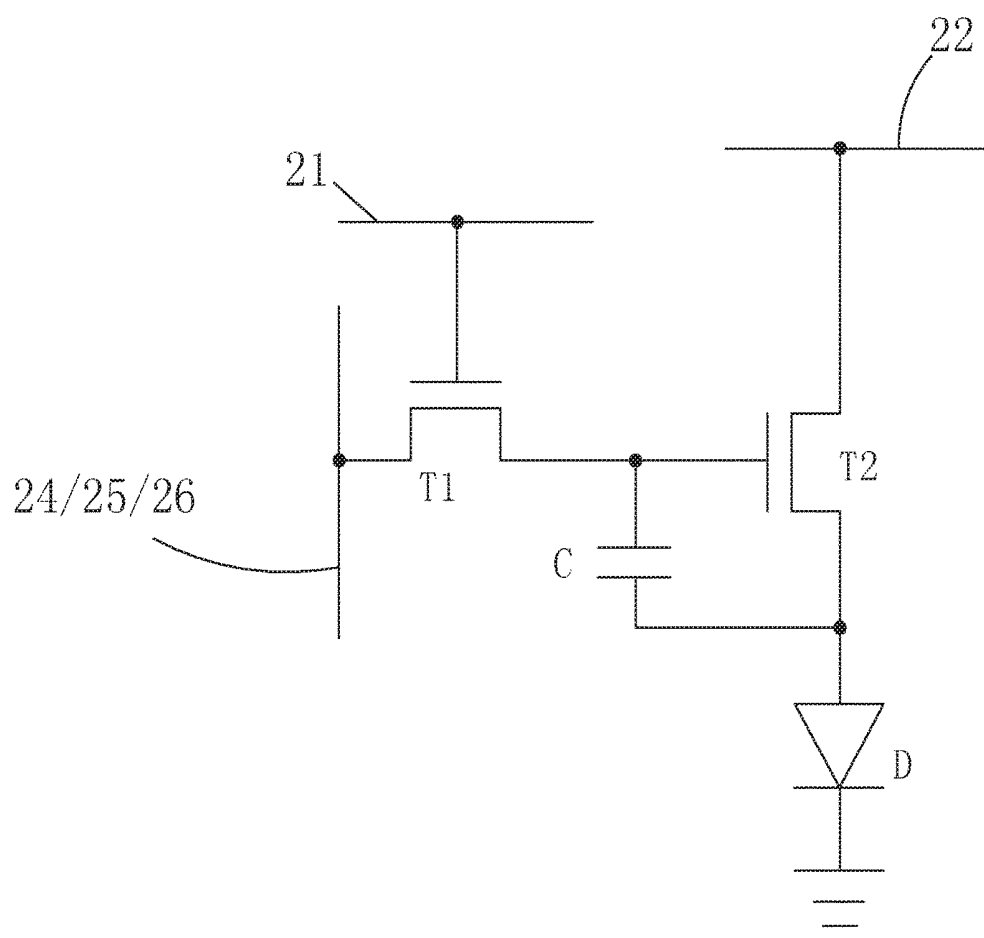


Fig. 5

TRANSPARENT OLED DISPLAY PANEL

FIELD OF THE INVENTION

[0001] The present application relates to a display technology field, and more particularly to a transparent OLED display panel.

BACKGROUND OF THE INVENTION

[0002] With the development of display technology, a variety of new technologies continue to emerge, transparent display technology because of its feature of transparent display panel and its unique application, has more and more people's attention.

[0003] A transparent display apparatus generally refers to a display that can form a transparent display state so that the viewer can see the image displayed in the display and the scene behind the display apparatus. Transparent display apparatus have many possible applications, such as windows for buildings or cars and shopping windows for shopping malls. In addition to the application of these large devices, small devices such as handheld tablet PCs can also benefit from transparent display apparatus, such as enabling users to view the map and be able to view the front scene through the display.

[0004] It is expected that most of the existing display market will be gradually replaced by transparent display, such as in the fields of architecture, advertising and public information. The transparent display is divided into a head-up display, a transparent liquid crystal display, LCD and a transparent organic light-emitting diode, OLED. In these transparent displays, the head-up display is realized by image projection, and transparent liquid crystal display and transparent OLED display is a true sense of the transparent display. And compared to the LCD display, its own characteristics of OLED display makes it more suitable for the production of transparent display.

[0005] As shown in FIG. 1, a transparent OLED display in the conventional technology includes a plurality of display pixels 100 and a plurality of transparent regions 200, the plurality of display pixels 100 arranged in an array type, one transparent region 200 is provided between each of the two adjacent columns of the display pixels 100, a second power supply line 300 is provided corresponding to each column of the display pixels 100, a scanning line 400 and a first power supply line 500 are provided corresponding to each row of display pixels 100; and each of the display pixels 100 includes red, green, and the blue sub-pixels 101, 102, 103 arranged sequentially along the column direction. A red data line 501 is provided corresponding to each column of the red sub-pixels 101, a green data line 502 is provided corresponding to each column of the green sub-pixels 102, a blue data line 503 is provided corresponding to each column of the blue sub-pixels 103, the second power supply line 300, the red data line 501, the green data line 502, and the blue data line 503 are located on the same layer and are arranged space apart from each other, and all of them extend downwards and need to be pass through the transparent region 200, resulting in excessive formation of the metal lines in the transparent region 200, making a decrease in the transmittance of the transparent region 200, and affecting the transmission effect.

SUMMARY OF THE INVENTION

[0006] The object of the present application is to provide a transparent OLED display panel which can reduce the area of the traces of the transparent region of the transparent OLED display panel and enhance the transmittance of the transparent OLED display panel to facilitate the development of the high resolution transparent OLED display panel.

[0007] In order to achieve the above object, the present application provides a transparent OLED display panel including: a plurality of display pixels arranged in an array type, each of the plurality of display pixels including a display region and a transparent region sequentially arranged along a vertical direction, each display region including a first, a second, and a third sub-pixels sequentially arranged along the horizontal direction;

[0008] a horizontal scanning line and a horizontal first power supply line electrically connected to a row of the display pixel is provided corresponding to each row of the display pixel, a vertical second power supply line electrically connected to the first power supply line is provided corresponding to each column of the display pixel, a first data line electrically connected to the first sub-pixel is provided corresponding to each column of the first sub-pixel, a second data line electrically connected to the second sub-pixel is provided corresponding to each column of the second sub-pixel, a third data line electrically connected to the third sub-pixel is provided corresponding to each column of the third sub-pixel;

[0009] the first power supply line and the scanning line are located in the first metal layer, the first data line and the second data line are located in the second metal layer stacked above the first metal layer, an insulating layer is provided between the first metal layer and the second metal layer;

[0010] the second power supply line including: a first extension portion and a first bridge portion, the first extension portion is located in the first metal layer, the first bridge portion is located in the second metal layer, the first bridge portion is electrically connected to the first extension portion through a first via hole in the insulating layer, and the second power supply line is insulated from and cross the scanning line by the first bridge portion; the third data line including a second extension portion and a second bridge portion, the second extension portion is located in the first metal layer, the second bridge portion is located in the second metal layer, the second bridge portion is electrically connected to the second extension portion through a second via hole in the insulating layer, and the third data line is insulated from and cross the first power supply line by the second bridge portion and the scanning line; and

[0011] in the transparent region, the first data line is insulated and stacked to the second power supply line, and the second data line is insulated and stacked to the third data line.

[0012] The first, second, and third sub-pixels are red, green, and blue sub-pixels, respectively.

[0013] Each of the sub-pixels including a first thin film transistor, a second thin film transistor, a capacitor, and an organic light emitting diode;

[0014] the gate of the first thin film transistor is electrically connected to the scanning line, the source is electrically connected to the data line corresponding to the sub-pixel, the drain is electrically connected to the gate of the second thin film transistor and one end of the capacitor; the drain of the

second thin film transistor is electrically connected to the first power supply line corresponding to the sub-pixel, the source is electrically connected to an anode of the organic light emitting diode; the anode of the organic light emitting diode is electrically connected to the other end of the capacitive, and a cathode is grounded.

[0015] The gate of the first thin film transistor, the gate of the second thin film transistor, and the one end of the capacitor are located in the first metal layer, the source and the drain of the first thin film transistor, the source and the drain of the second thin film transistor, and the other end of the capacitor are located in the second metal layer.

[0016] The insulating layer including a gate insulating layer and an interlayer insulating layer; and an active layer is provided on the gate insulating layer corresponding to the positions of the gate of the first thin film transistor and the gate of the second thin film transistor, and the interlayer insulating layer covers the active layer and the gate insulating layer.

[0017] The source and drain of the first thin film transistor and the source and the drain of the second thin film transistor are in contact with both ends of the corresponding active layer through the two third via holes, respectively.

[0018] The materials of the first metal layer and the second metal layer are both of one or a combination of Aluminum, Molybdenum, and Titanium.

[0019] The material of the insulating layer is one or the combination of Silicon Oxide and Silicon Nitride.

[0020] The first data line and the second power supply line are located on the left edge side of the display pixel, the second data line and the third data line are located on the right edge side of the display pixel.

[0021] The present application further provides a transparent OLED display panel, including: a plurality of display pixels arranged in an array type, each of the plurality of display pixels including a display region and a transparent region sequentially arranged along a vertical direction, each display region including a first, a second, and a third sub-pixels sequentially arranged along the horizontal direction;

[0022] a horizontal scanning line and a horizontal first power supply line electrically connected to a row of the display pixel is provided corresponding to each row of the display pixel, a vertical second power supply line electrically connected to the first power supply line is provided corresponding to each column of the display pixel, a first data line electrically connected to the first sub-pixel is provided corresponding to each column of the first sub-pixel, a second data line electrically connected to the second sub-pixel is provided corresponding to each column of the second sub-pixel, a third data line electrically connected to the third sub-pixel is provided corresponding to each column of the third sub-pixel;

[0023] the first power supply line and the scanning line are located in the first metal layer, the first data line and the second data line are located in the second metal layer stacked above the first metal layer, an insulating layer is provided between the first metal layer and the second metal layer;

[0024] the second power supply line including: a first extension portion and a first bridge portion, the first extension portion is located in the first metal layer, the first bridge portion is located in the second metal layer, the first bridge portion is electrically connected to the first extension portion

through a first via hole in the insulating layer, and the second power supply line is insulated from and cross the scanning line by the first bridge portion; the third data line including a second extension portion and a second bridge portion, the second extension portion is located in the first metal layer, the second bridge portion is located in the second metal layer, the second bridge portion is electrically connected to the second extension portion through a second via hole in the insulating layer, and the third data line is insulated from and cross the first power supply line by the second bridge portion and the scanning line;

[0025] in the transparent region, the first data line is insulated and stacked to the second power supply line, and the second data line is insulated and stacked to the third data line.

[0026] wherein the first, second, and third sub-pixels are red, green, and blue sub-pixels, respectively;

[0027] wherein each of the sub-pixels including a first thin film transistor, a second thin film transistor, a capacitor, and an organic light emitting diode;

[0028] the gate of the first thin film transistor is electrically connected to the scanning line, the source is electrically connected to the data line corresponding to the sub-pixel, the drain is electrically connected to the gate of the second thin film transistor and one end of the capacitor; the drain of the second thin film transistor is electrically connected to the first power supply line corresponding to the sub-pixel, the source is electrically connected to an anode of the organic light emitting diode; the anode of the organic light emitting diode is electrically connected to the other end of the capacitive, and a cathode is grounded.

[0029] The advantageous Effects of the present application: the present application provides a transparent OLED display panel, by providing the second power supply line and the first data line in the transparent region of the transparent OLED display panel in the first metal layer and the second metal layer, respectively, so that the two are insulated and arranged in a stacking manner, and the second data line and the third data line are respectively provided in the first metal layer and the second metal layer so that the two are insulated and arranged in a stacking manner, which the area of the traces of the transparent region of the transparent OLED display panel can be greatly reduced compared to the interval arrangement in the conventional technology, the transmittance of the transparent OLED display panel is enhanced and to facilitate the development of the high resolution transparent OLED display panel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] In order to more clearly illustrate the embodiments of the present application or prior art, the following figures will be described in the embodiments are briefly introduced. It is obvious that the drawings are merely some embodiments of the present application, those of ordinary skill in this field can obtain other figures according to these figures without paying the premise.

[0031] FIG. 1 is a schematic structural view of a transparent OLED display panel in the conventional technology;

[0032] FIG. 2 is a schematic structural view of a transparent OLED display panel of the present application;

[0033] FIG. 3 is a cross-sectional view corresponding to the A-A site illustrated in FIG. 2;

[0034] FIG. 4 is a cross-sectional view corresponding to the B-B site illustrated in FIG. 2; and

[0035] FIG. 5 is a circuit diagram of a sub-pixel of the transparent OLED display panel of the present application.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0036] Embodiments of the present application are described in detail with the technical matters, structural features, achieved objects, and effects with reference to the accompanying drawings as follows. It is clear that the described embodiments are part of embodiments of the present application, but not all embodiments. Based on the embodiments of the present application, all other embodiments to those of ordinary skill in the premise of no creative efforts acquired should be considered within the scope of protection of the present application.

[0037] Specifically, the terminologies in the embodiments of the present application are merely for describing the purpose of the certain embodiment, but not to limit the invention.

[0038] Referring to FIG. 2, the present application provides a transparent OLED display panel including a plurality of display pixels 1 arranged in an array type, each of the plurality of display pixels 1 includes a display region 11 and a transparent region 12 sequentially arranged along a vertical direction, a first, a second, and a third sub-pixels 111, 112, and 113 are provided in each of the display region 11 and sequentially arranged along the horizontal direction.

[0039] Specifically, a horizontal scanning line 21 and a horizontal first power supply line 22 electrically connected to each row of the display pixel 1 is provided corresponding to each row of the display pixel 1, a vertical second power supply line 23 electrically connected to the first power supply line 22 is provided corresponding to each column of the display pixel 1, a first data line 24 electrically connected to the first sub-pixel 111 is provided corresponding to each column of the first sub-pixel 111, a second data line 25 electrically connected to the second sub-pixel 112 is provided corresponding to each column of the second sub-pixel 112, a third data line 26 electrically connected to the third sub-pixel 113 is provided corresponding to each column of the third sub-pixel 113;

[0040] The first power supply line 22 and the scanning line 21 are located in the first metal layer 31, and the first data line 24 and the second data line 25 are located in the second metal layer 32 stacked above the first metal layer 31, an insulating layer 33 is provided between the first metal layer 31 and the second metal layer 32;

[0041] The second power supply line 23 includes a first extension portion 231 and a first bridge portion 232, the first extension portion 231 is located in the first metal layer 31, the first bridge portion 232 is located in the second metal layer 32, the first bridge portion 232 is electrically connected to the first extension portion 231 through a first via hole 333 in the insulating layer 33, and the second power supply line 23 is insulated from and cross the scanning line 21 by the first bridge portion 232. The third data line 26 includes a second extension portion 261 and a second bridge portion 262, the second extension portion 261 is located in the first metal layer 31, the second bridge portion 262 is located in the second metal layer 32, the second bridge portion 262 is electrically connected to the second extension portion 261 through a second via hole 334 in the insulating layer 33, and

the third data line 26 is insulated from and cross the first power supply line 22 by the second bridge portion 262 and the scanning line 21;

[0042] In the transparent region 12, the first data line 24 is insulated from and stacked arranged to the second power supply line 23, and the second data line 25 is insulated from and stacked arranged to the third data line 26.

[0043] Specifically, the plurality of the display pixels 1 arranged in the array type are disposed on a transparent substrate 10, the transparent substrate 10 is specifically selected from a glass substrate or a plastic substrate, the first, second, and third sub-pixels 111, 112, 113 are red, green, and blue sub-pixels, respectively.

[0044] Further, referring to FIG. 5, each of the sub-pixels including the first, second, and third sub-pixels 111, 112, 113 is provided with a first thin film transistor T1, a second thin film transistor T2, a capacitor C, and an organic light emitting diode D;

[0045] Wherein the gate of the first thin film transistor T1 is electrically connected to the scanning line 21, the source is electrically connected to the data line corresponding to the sub-pixel, the drain is electrically connected to the gate of the second thin film transistor T2 and one end of the capacitor C; the drain of the second thin film transistor T2 is electrically connected to the first power supply line 22 corresponding to the sub-pixel, the source is electrically connected to the anode of the organic light emitting diode D; the anode of the organic light emitting diode D is electrically connected to the other end of the capacitive C, and the cathode is grounded.

[0046] Specifically, the gate of the first thin film transistor T1, the gate of the second thin film transistor T2, and the one end of the capacitor C are located in the first metal layer 31, the source and the drain of the first thin film transistor T1, the source and the drain of the second thin film transistor T2, and the other end of the capacitor C are located in the second metal layer 32, and the insulating layer 33 includes a gate insulating layer 331 and an interlayer insulating layer 332, the gate insulating layer 331 is provided with an active layer 34 at positions corresponding to the gate of the first thin film transistor T1 and the gate of the second thin film transistor T2, and the interlayer insulating layer 332 covers the active layer 34 and the gate insulating layer 331, the source and drain of the first thin film transistor T1 and the source and the drain of the second thin film transistor T2 are in contact with both ends of the corresponding active layer 34 through the two third via holes 335, respectively.

[0047] Specifically, the third data line 26 is electrically connected to the source of the first thin film transistor T1 of the third sub-pixel 113 through the second bridge portion 262.

[0048] Further, a planarization layer, the anode of the organic light emitting diode D, the pixel definition layer, and the cathode of the organic light emitting diode D is stacking provided on the second metal layer 32 from the lower side to the upper side, a pixel defining groove is formed in the pixel defining layer, the anode of the organic light emitting diode D and the cathode of the organic light emitting diode D are formed on the upper and lower sides of the pixel defining groove, the organic light emitting layer of the organic light emitting diode D formed within the pixel defining groove, the anode of the organic light emitting diode D is electrically connected to the source of the second

thin film transistor T2 and the one end of the capacitor C through the via in the planarization layer.

[0049] Specifically, the drain of the second thin film transistor T2 is electrically connected to the first power supply line 22 through a through hole penetrating the insulating layer 33, the drain of the first thin film transistor T1 is electrically connected to gate of the second thin film transistor T2 through a through hole penetrating the insulating layer 33.

[0050] It is to be noted that the gate of the first thin film transistor T1 acquires a scan control signal from the scanning line 21, the source of the first thin film transistor T1 acquires a data signal from the first data line 24 or the second data line 25 or the third data line 26, the gate of the second thin film transistor T2 acquires a data signal from the drain of the first thin film transistor T1, and the drain of the second thin film transistor T2 acquires a power supply signal from the first power supply line 22 to drive the organic light emitting diode D to emit light.

[0051] Preferably, the materials of the first metal layer 31 and the second metal layer 32 are both of one or combination of Aluminum, Molybdenum, and Titanium. The material of the insulating layer 33 is one or the combination of Silicon Oxide and Silicon Nitride. Preferably, the first data line 24 and the second power supply line 23 are located on the left edge side of the display pixel 1, the second data line 25 and the third data line 26 are located on the right edge side of the display pixel 1, so that the central region of the transparent region 12 of the display pixel 1 no longer has any metal traces passed, greatly enhancing the transmittance of the transparent OLED display panel, and to facilitate the development of the high resolution transparent OLED display panel.

[0052] In view of the above, the present application provides a transparent OLED display panel in which a second power supply line and a first data line in the transparent region of the transparent OLED display panel are provided to the first metal layer and the second metal layer, respectively, so that the two layers are insulated and stacked. Simultaneously, the second data line and the third data line are also provided in the first metal layer and the second metal layer, respectively, so that the two layers are insulated and stacked, respectively, compared to the interval arrangement in the conventional technology, the area of the traces of the transparent region of the transparent OLED display panel can be greatly reduced, the transmittance of the transparent OLED display panel is enhanced and to facilitate the development of the high resolution transparent OLED display panel.

[0053] Above are embodiments of the present application, which does not limit the scope of the present application. Any modifications, equivalent replacements or improvements within the spirit and principles of the embodiment described above should be covered by the protected scope of the invention.

What is claimed is:

1. A transparent OLED display panel, comprising: a plurality of display pixels arranged in an array type, each of the plurality of display pixels comprising a display region and a transparent region sequentially arranged along a vertical direction, each display region comprising a first, a second, and a third sub-pixels sequentially arranged along the horizontal direction;

a horizontal scanning line and a horizontal first power supply line electrically connected to a row of the display pixel is provided corresponding to each row of the display pixel, a vertical second power supply line electrically connected to the first power supply line is provided corresponding to each column of the display pixel, a first data line electrically connected to the first sub-pixel is provided corresponding to each column of the first sub-pixel, a second data line electrically connected to the second sub-pixel is provided corresponding to each column of the second sub-pixel, a third data line electrically connected to the third sub-pixel is provided corresponding to each column of the third sub-pixel;

the first power supply line and the scanning line are located in the first metal layer, the first data line and the second data line are located in the second metal layer stacked above the first metal layer, an insulating layer is provided between the first metal layer and the second metal layer;

the second power supply line comprising: a first extension portion and a first bridge portion, the first extension portion is located in the first metal layer, the first bridge portion is located in the second metal layer, the first bridge portion is electrically connected to the first extension portion through a first via hole in the insulating layer, and the second power supply line is insulated from and cross the scanning line by the first bridge portion; the third data line comprising a second extension portion and a second bridge portion, the second extension portion is located in the first metal layer, the second bridge portion is located in the second metal layer, the second bridge portion is electrically connected to the second extension portion through a second via hole in the insulating layer, and the third data line is insulated from and cross the first power supply line by the second bridge portion and the scanning line; and

in the transparent region, the first data line is insulated and stacked to the second power supply line, and the second data line is insulated and stacked to the third data line.

2. The transparent OLED display panel according to claim 1, wherein the first, second, and third sub-pixels are red, green, and blue sub-pixels, respectively.

3. The transparent OLED display panel according to claim 1, wherein each of the sub-pixels comprising a first thin film transistor, a second thin film transistor, a capacitor, and an organic light emitting diode;

the gate of the first thin film transistor is electrically connected to the scanning line, the source is electrically connected to the data line corresponding to the sub-pixel, the drain is electrically connected to the gate of the second thin film transistor and one end of the capacitor; the drain of the second thin film transistor is electrically connected to the first power supply line corresponding to the sub-pixel, the source is electrically connected to an anode of the organic light emitting diode; the anode of the organic light emitting diode is electrically connected to the other end of the capacitive, and a cathode is grounded.

4. The transparent OLED display panel according to claim 3, wherein the gate of the first thin film transistor, the gate of the second thin film transistor, and the one end of the capacitor are located in the first metal layer, the source and

the drain of the first thin film transistor, the source and the drain of the second thin film transistor, and the other end of the capacitor are located in the second metal layer.

5. The transparent OLED display panel according to claim 4, wherein the insulating layer comprising a gate insulating layer and an interlayer insulating layer; and

an active layer is provided on the gate insulating layer corresponding to the positions of the gate of the first thin film transistor and the gate of the second thin film transistor, and the interlayer insulating layer covers the active layer and the gate insulating layer.

6. The transparent OLED display panel according to claim 5, wherein the source and drain of the first thin film transistor and the source and the drain of the second thin film transistor are in contact with both ends of the corresponding active layer through the two third via holes, respectively.

7. The transparent OLED display panel according to claim 1, wherein the materials of the first metal layer and the second metal layer are both of one or a combination of Aluminum, Molybdenum, and Titanium.

8. The transparent OLED display panel according to claim 1, wherein the material of the insulating layer is one or the combination of Silicon Oxide and Silicon Nitride.

9. The transparent OLED display panel according to claim 1, wherein the first data line and the second power supply line are located on the left edge side of the display pixel, the second data line and the third data line are located on the right edge side of the display pixel.

10. A transparent OLED display panel, comprising: a plurality of display pixels arranged in an array type, each of the plurality of display pixels comprising a display region and a transparent region sequentially arranged along a vertical direction, each display region comprising a first, a second, and a third sub-pixels sequentially arranged along the horizontal direction;

a horizontal scanning line and a horizontal first power supply line electrically connected to a row of the display pixel is provided corresponding to each row of the display pixel, a vertical second power supply line electrically connected to the first power supply line is provided corresponding to each column of the display pixel, a first data line electrically connected to the first sub-pixel is provided corresponding to each column of the first sub-pixel, a second data line electrically connected to the second sub-pixel is provided corresponding to each column of the second sub-pixel, a third data line electrically connected to the third sub-pixel is provided corresponding to each column of the third sub-pixel;

the first power supply line and the scanning line are located in the first metal layer, the first data line and the second data line are located in the second metal layer stacked above the first metal layer, an insulating layer is provided between the first metal layer and the second metal layer;

the second power supply line comprising: a first extension portion and a first bridge portion, the first extension portion is located in the first metal layer, the first bridge portion is located in the second metal layer, the first bridge portion is electrically connected to the first extension portion through a first via hole in the insulating layer, and the second power supply line is insulated from and cross the scanning line by the first

bridge portion; the third data line comprising a second extension portion and a second bridge portion, the second extension portion is located in the first metal layer, the second bridge portion is located in the second metal layer, the second bridge portion is electrically connected to the second extension portion through a second via hole in the insulating layer, and the third data line is insulated from and cross the first power supply line by the second bridge portion and the scanning line;

in the transparent region, the first data line is insulated and stacked to the second power supply line, and the second data line is insulated and stacked to the third data line. wherein the first, second, and third sub-pixels are red, green, and blue sub-pixels, respectively;

wherein each of the sub-pixels comprising a first thin film transistor, a second thin film transistor, a capacitor, and an organic light emitting diode;

the gate of the first thin film transistor is electrically connected to the scanning line, the source is electrically connected to the data line corresponding to the sub-pixel, the drain is electrically connected to the gate of the second thin film transistor and one end of the capacitor; the drain of the second thin film transistor is electrically connected to the first power supply line corresponding to the sub-pixel, the source is electrically connected to an anode of the organic light emitting diode; the anode of the organic light emitting diode is electrically connected to the other end of the capacitor, and a cathode is grounded.

11. The transparent OLED display panel according to claim 10, wherein the gate of the first thin film transistor, the gate of the second thin film transistor, and the one end of the capacitor are located in the first metal layer, the source and the drain of the first thin film transistor, the source and the drain of the second thin film transistor, and the other end of the capacitor are located in the second metal layer.

12. The transparent OLED display panel according to claim 11, wherein the insulating layer comprising a gate insulating layer and an interlayer insulating layer; and

an active layer is provided on the gate insulating layer corresponding to the positions of the gate of the first thin film transistor and the gate of the second thin film transistor, and the interlayer insulating layer covers the active layer and the gate insulating layer.

13. The transparent OLED display panel according to claim 12, wherein the source and drain of the first thin film transistor and the source and the drain of the second thin film transistor are in contact with both ends of the corresponding active layer through the two third via holes, respectively.

14. The transparent OLED display panel according to claim 10, wherein the materials of the first metal layer and the second metal layer are both of one or a combination of Aluminum, Molybdenum, and Titanium.

15. The transparent OLED display panel according to claim 10, wherein the material of the insulating layer is one or the combination of Silicon Oxide and Silicon Nitride.

16. The transparent OLED display panel according to claim 10, wherein the first data line and the second power supply line are located on the left edge side of the display pixel, the second data line and the third data line are located on the right edge side of the display pixel.

专利名称(译)	透明OLED显示屏		
公开(公告)号	US20180233550A1	公开(公告)日	2018-08-16
申请号	US15/509198	申请日	2017-02-16
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
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[标]发明人	HAN BAIXIANG		
发明人	HAN, BAIXIANG		
IPC分类号	H01L27/32		
CPC分类号	H01L27/3276 H01L27/3211		
优先权	201710038290.2 2017-01-19 CN		
其他公开文献	US10249698		
外部链接	Espacenet USPTO		

摘要(译)

本申请提供了一种透明OLED显示面板。通过在第一金属层和第二金属层中的透明OLED显示面板的透明区域中分别提供第二电源线和第一数据线，并使两个绝缘层以堆叠方式布置，并且第二数据线和第三数据线分别设置在第一金属层和第二金属层中，并且使得两个绝缘层以堆叠方式布置，与传统技术中的间隔布置相比，透明区域的迹线的面积透明OLED显示面板的透明度可以大大降低，透明OLED显示面板的透光率提高，便于高分辨率透明OLED显示面板的开发。

